What is claimed is:

1. A semiconductor integrated circuit including an insulated gate field effect transistor of which gate electrode comprising:

(a) a first region composed of at least a first IV group element and a second IV group element which are different from each other, and formed on an insulated gate film of a semiconductor substrate; and

(b) a second region composed of the first IV group element and formed on the first region.

2. The semiconductor integrated circuit of claim 1, wherein the first region of the gate electrode has a composition ratio of the second IV group element gradually reduced in accordance with a distance from the insulated gate film.

3. The semiconductor integrated circuit of claim 1, wherein the first region of the gate electrode has a composition ratio of the second IV group element stepwise reduced in accordance with a distance from the insulated gate film.

4. A semiconductor integrated circuit comprising:

(a) an insulated gate field effect transistor including a gate electrode which is provided with a first region composed of at least a first IV group element and a second IV group element which are different from each other and formed on an insulated gate film on a semiconductor substrate, and a second region composed of the first IV group element and formed on the first region; and

(b) a silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second IV group element.

5. The semiconductor integrated circuit of claim 4, wherein the first IV group element of the gate electrode is Si

(silicon), the second IV group element of the gate electrode is Ge (germanium), and the silicide electrode is composed of $CoSi_y$ or $TiSi_y$ layer which is substantially free from Ge.

6. The semiconductor integrated circuit of claim 5, wherein the first region of the gate electrode has a thickness larger than a width of a depletion layer of the gate electrode composed of Si.

7. The semiconductor integrated circuit of claim 6, wherein a composition ratio of Ge of the first region of the gate electrode is at least 0.1 or larger.

8. The semiconductor integrated circuit of claim 7, wherein the gate electrode contains at least B (boron).

9. The semiconductor integrated circuit of claim 7, wherein the gate electrode contains at least As (arsenic).

10. The semiconductor integrated circuit of claim 4, wherein the first IV group element of the gate electrode is Si, the second IV group element of the gate electrode is C (carbon), and the silicide electrode is composed of a $CoSi_y$ or $TiSi_y$ layer which is substantially free of C.

11. A semiconductor integrated circuit comprising:

(a) an insulated gate field effect transistor including a gate electrode which is provided with a first region composed of at least a first IV group element and a second IV group element which are different from each other, and formed on an insulated gate film on a semiconductor substrate, and a second region composed of a multiple element compound including at least the first and second IV group elements and metal, and formed on the first region; and

(b) a silicide electrode formed in contact with the second region of the gate electrode, composed of the first IV group

element and metal, and being substantially free from the second IV group element.

12. A method of manufacturing a semiconductor integrated circuit having an insulated gate field effect transistor, wherein a gate electrode of the insulated gate field effect transistor is manufactured by the steps of:

(a) forming, on an insulated gate film on a semiconductor substrate, a first region composed of at least a first IV group element and a second IV group element which are different from each other, and forming, on the first region, a second region composed of the first IV group element; and

(b) forming a silicide electrode through silicidation of at least a part of the second region of the gate electrode.

13. A method of manufacturing a semiconductor integrated circuit including insulated gate field effect transistors, comprising the steps of:

(a) forming, on a gate insulated film on a semiconductor substrate, a first region composed of at least a first IV group element and a second IV group element which are different from each other, and forming, on the first region, a second region composed of the first IV group element, thereby obtaining a first gate electrode for an insulated gate field effect transistor of a first conductive channel type;

(b) forming, on the insulated gate film of the semiconductor substrate at a region besides the first conductive channel type insulated field effect transistor, a third region composed of a third IV group element and a fourth IV group element which are different from each other, and forming, on the third region, a fourth region composed of the third IV group element, thereby obtaining a second gate electrode for an insulated gate field effect transistor of a second conductive channel type which has a conductive type opposite to that of the first conductive channel type; and

(c) introducing a first conductive impurity into the first

electrode and a second conductive impurity into the second gate electrode; and

(d) forming a silicide electrode through silicidation of at least a part of the second region of the first gate electrode and at least a part of the fourth region of the second region into silicide.

14. The method of claim 13, wherein the step (c) is the same as a step of introducing a first conductive impurity into a source or drain electrode of the first conductive channel type insulated gate field effect transistor, and the step (d) is the same as a step of introducing a second conductive impurity into the source or drain electrode of the second conductive channel type insulated gate field effect transistor.

15. A semiconductor integrated circuit comprising:

(a) a semiconductor region of a first conductive type;

(b)an epitaxial growth layer formed on the semiconductor region and including a first region composed of at least a first IV group element and a second IV group element which are different from each other and a second region composed of the first IV group element; and

(c) a silicide electrode formed on the second region of the epitaxial growth layer.

16. The semiconductor integrated circuit of claim 15, wherein the semiconductor region is a source or drain electrode of the insulated gate field effect transistor, and the epitaxial growth layer is an elevated source or drain electrode.

17. The semiconductor integrated circuit of claim 16, wherein the first IV group element of the elevated source or drain electrode is Si, the second IV group element of the elevated source or drain electrode is Ge, and the silicide electrode is made of a $CoSi_y$ or $TiSi_y$ layer which is substantially free from Ge.

18. The semiconductor integrated circuit of claim 17, wherein a composition ratio of Ge in the first region of the elevated source or drain electrode is at least 0.1 or more, and a thickness of the first region is at least 2nm from the semiconductor region.

19. The semiconductor integrated circuit of claim 18, wherein the elevated source or drain electrode contains at least B.

20. The semiconductor integrated circuit of claim 18, wherein the elevated source or drain electrode contains at least As.

21. The semiconductor integrated circuit of claim 16, wherein the first IV group element of the elevated source or drain electrode is Si, the second IV group element of the elevated source or drain electrode is C, and the silicide electrode made of a $CoSi_y$ or $TiSi_y$ layer which is substantially free from C.

22. A method of forming a semiconductor integrated circuit comprising the steps of:

(a) forming a main electrode of an insulated gate field effect transistor;

(b) forming, on the main electrode, a first region composed of a first IV group element and a second IV group element which are different from each other, and forming, on the first region, a second region composed of the first IV group element, thereby forming an elevated electrode; and

(c) forming a silicide electrode through silicidation of a part of the second region of the elevated electrode.

23. A semiconductor integrated circuit comprising:

(a) an insulated gate field effect transistor including a gate electrode provided with a first region which is composed of at least a first IV group element and a second IV group element of different kinds and formed on an insulated gate film of a

semiconductor substrate, and a second region which is composed of the first IV group element and formed on the first region, and a main electrode;

(b) an elevated electrode formed on the main electrode, and having a third region composed of a third IV group element and a fourth IV group element which are different from each other and a fourth region formed on the third region and composed of the third IV group element;

(c) a first silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second IV group element; and

(d) a second silicide electrode formed in contact with the fourth region of the elevated electrode, and being substantially free from the fourth IV group element.

24. A method of forming a semiconductor integrated circuit including an insulated gate field effect transistor, comprising the steps of:

(a) forming, on an insulated gate film on a semiconductor substrate, a first region composed of a first IV group element and a second IV group element of different types, and forming, on the first region, a second region composed of the first IV group element, and forming a main electrode, thereby obtaining the insulated gate field effect transistor;

(b) forming, on the main electrode, a third region composed of a third IV group element and a fourth IV group element which are different from each other, and forming, on the third region, a fourth region composed o the third IV group element;

(c) forming a first silicide electrode through silicidation of at least a part of the second region of the gate electrode, the silicide electrode being substantially free from the second IV group element; and

(d) forming a second silicide electrode through silicidation of at least a part of the fourth region of the elevated electrode simultaneously with the step (c), the second silicide electrode being substantially free from the fourth IV

group element.

25. The semiconductor integrated circuit of claim 1, wherein a layer is added between the insulated gate film and the first region of the gate electrode, is thinner than the first region, and is composed of the first IV group element or the second IV group element.

26. The semiconductor integrated circuit of claim 4, wherein a layer is added between the insulated gate film and the first region of the gate electrode, is thinner than the first region, and is composed of the first IV group element or the second IV group element.

27. The semiconductor integrated circuit of claim 11, wherein a layer is added between the insulated gate film and the first region of the gate electrode, is thinner than the first region, and is composed of the first IV group element or the second IV group element.